

AD-A239 639



IDENTIFICATION PAGE

Form Approved

OMB No. 0704-0188

estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering the collection of information, Send comments regarding this burden estimate or any other aspect of this burden to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Avenue, Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503

REPORT DATE July 26, 1991		3. REPORT TYPE AND DATES COVERED Final 1 Nov 87 - 31 May 91	
4. TITLE AND SUBTITLE Limited Reaction Processing for Semiconductor Materials Preparation		5. FUNDING NUMBERS DAAL03-88-K-0020 DAAL03-88-G-0001	
6. AUTHOR(S) J. L. Hoyt			
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) J. F. Gibbons, Principal Investigator Stanford University Stanford, CA 94305		8. PERFORMING ORGANIZATION REPORT NUMBER	
9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES) U. S. Army Research Office P. O. Box 12211 Research Triangle Park, NC 27709-2211		10. SPONSORING / MONITORING AGENCY REPORT NUMBER ARO 25611.1-EL ARO 25675.1-EL-EQ	
11. SUPPLEMENTARY NOTES The view, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.			
12a. DISTRIBUTION / AVAILABILITY STATEMENT Approved for public release; distribution unlimited.		12b. DISTRIBUTION CODE AUG 20 1991	
13. ABSTRACT (Maximum 200 words) This document is the final report for U.S. Army Research Office contract number DAAL03-88-K-0020 and associated equipment grant DAAL03-88-G-0001. Limited Reaction Processing (LRP) is a layer deposition technique based upon a combination of rapid thermal processing (RTP) and chemical vapor deposition. Under this contract, the versatility of LRP has been demonstrated in research on epitaxial growth in three different materials systems: Column IV (Si/Si _{1-x} Ge _x), III-V, and II-VI semiconductors. This work has spurred research at several other laboratories in the area of epitaxial growth and applications involving RTP techniques, particularly in the Si _{1-x} Ge _x materials system. We have fabricated the first CVD-grown Si/Si _{1-x} Ge _x heterojunction bipolar transistors using this technique, with maximum oscillation frequencies on the order of 40 GHz. In the III-V area, we have explored arsine alternative sources for GaAs epitaxy which greatly improve the safety of MOCVD. We have also developed a new atomic layer growth technique by combining LRP with an alternating gas-pulse method.			
14. SUBJECT TERMS		15. NUMBER OF PAGES 10	
16. PRICE CODE		17. SECURITY CLASSIFICATION OF REPORT UNCLASSIFIED	
18. SECURITY CLASSIFICATION OF THIS PAGE UNCLASSIFIED		19. SECURITY CLASSIFICATION OF ABSTRACT UNCLASSIFIED	
20. LIMITATION OF ABSTRACT UL			

91 8 19 085

LIMITED REACTION PROCESSING FOR SEMICONDUCTOR MATERIALS PREPARATION

FINAL REPORT

J. L. Hoyt

July 1991

J. F. Gibbons
Principal Investigator

U. S. Army Research Office

Stanford University
Stanford, California 94305



Accession For	
NTIS GRA&I	
ERIC 178	
Unannounced	
Justification	
By	
Distribution	
Availability Codes	
Dist	Availability Code Special
A-1	

Approved for public release: distribution unlimited

THE VIEWS, OPINIONS, AND/OR FINDINGS CONTAINED IN THIS REPORT ARE
THOSE OF THE AUTHOR(S) AND SHOULD NOT BE CONSTRUED AS AN
OFFICIAL DEPARTMENT OF THE ARMY POSITION, POLICY, OR DECISION,
UNLESS SO DESIGNATED BY OTHER DOCUMENTATION.

FOREWORD

This document is the final report for U.S. Army Research Office contract number DAAL03-88-K-0020 and associated equipment grant DAAL03-88-G-0001, which correspond to the proposal entitled **Limited Reaction Processing for Semiconductor Materials Preparation**. Limited Reaction Processing (LRP) is a layer deposition technique based upon a combination of rapid thermal processing (RTP) and chemical vapor deposition. Under this contract, the versatility of LRP has been demonstrated in research on epitaxial growth in three different materials systems: Column IV (Si/Si_{1-x}Ge_x), III-V, and II-VI semiconductors. This work has spurred research at several other laboratories in the area of epitaxial growth and applications involving RTP techniques, particularly in the Si/Si_{1-x}Ge_x materials system.

The problems addressed in the research performed under this contract fall into two broad categories:

1. understanding the fundamental relationships between the conditions for the materials growth/processing and the resulting material and electrical characteristics of the epitaxial layers (enabling processes to be developed which optimize device performance), and
2. exploring in detail promising new device applications which utilize the unique structures fabricated by this technique (e.g. basic device physics of the Si/Si_{1-x}Ge_x heterojunction bipolar transistor).

This report constitutes a brief summary of research performed under the above contract. Part 1 contains a summary of the most important results including references to publications. Part 2 is a complete list of publications resulting from this contract period. Parts 3 and 4 list participating scientific personnel and inventions.

Part 1

Summary of the Research

The following three sections contain a summary of the most important results of the research performed under this contract. Research on epitaxial growth has been conducted using three LRP reactors fabricated at Stanford. These are dedicated to Column IV, III-V, and II-VI materials. The II-VI reactor was constructed as part of this contract. The other two machines were upgraded in order to perform this research. The emphasis of the work on Column IV materials has been the fabrication and analysis of Si/Si_{1-x}Ge_x heterojunction bipolar transistors, as well as understanding the fundamental materials properties of these strained layer structures. In the III-V area we have performed a detailed analysis of interrupted-growth interfaces. In II-VI materials growth, the major problem to be addressed is obtaining control over doping, composition, and thickness uniformity during growth. A new technique, which is a combination of LRP and atomic layer epitaxy has been explored.

1.1 Column IV Highlights

The following is a brief list of achievement highlights in our work on Si_{1-x}Ge_x/Si growth, and heterojunction bipolar transistor device applications. In this work we utilized the facilities of the Solid State Lab, Stanford Center for Integrated Systems, and the Center for Materials Research. In addition, much of the work was carried out in collaboration with Hewlett-Packard Circuit Technology R&D, in Palo Alto, CA.

- fabrication and analysis of the first Si/Si_{1-x}Ge_x heterojunction bipolar transistors (HBTs) produced in CVD-grown material. HBTs with moderately doped bases ($\approx 7 \times 10^{18} \text{ cm}^{-3}$) and emitter areas of $30 \times 30 \mu\text{m}^2$ have current gains of 250 to 400, in the range of 1nA up to 10 mA. We also found:
 - nearly ideal current characteristics
 - measured valence band offsets in good agreement with published calculations
 - the first quantitative measurements of the effects of strain relaxation on band offsets and HBT device performance
- fabrication and analysis of fine geometry HBTs with heavily doped (up to 10^{20} cm^{-3}) Si_{1-x}Ge_x base layers. Although relatively simple device structures were used, a cut-off frequency, F_t of approximately 28 GHz and F_{max} of approximately 35 GHz was achieved. This is the highest F_{max} published for Si/Si_{1-x}Ge_x HBTs to date.
- demonstration of selective growth of Si and Si_{1-x}Ge_x on oxide patterned wafers. Selectively-grown p-Si_{1-x}Ge_x/n-Si diodes were fabricated. [*Selective epitaxial growth provides an important opportunity for reducing parasitics*].

- measured misfit dislocation velocities using hot-stage transmission electron microscopy. Velocities are similar for LRP and MBE grown layers.
- complete analysis of the effects of oxygen doping on the mechanical and electrical characteristics of $\text{Si}_{1-x}\text{Ge}_x$ layers. A high concentration of oxygen ($\approx 2 \times 10^{20} \text{ cm}^{-3}$) produces:
 - substantial enhancement in thermal stability
 - degradation of minority carrier lifetimes
- development of a new technique for extraction of minority carrier lifetimes in very thin $\text{Si}_{1-x}\text{Ge}_x$ layers.
- performed experiments which contribute to the understanding of misfit dislocation formation:
 - an epitaxial Si cap (emitter) inhibits misfit dislocation formation during high temperature annealing (joint HP/SU patent application).
 - selective growth of SiGe in small windows on oxide-patterned wafers results in fewer dislocations (joint HP/SU patent application).
 - $2 \times 10^{20} \text{ cm}^{-3}$ oxygen slows dislocation formation during annealing and increases the thickness to which strained layers can be grown before the onset of misfit dislocation formation.
 - during growth, the onset of misfit dislocation formation is comparable in MBE and LRP-grown films.

1.2 III-V Highlights

In the past, our III-V research has focused on the growth of GaAs and AlGaAs using metal organic chemical vapor deposition (MOCVD). This work has several unique features which distinguish it from other studies, including: (1) organometallic arsenic sources are used in place of arsine, (2) the quartz reaction chamber can be configured for precracking of the Column V precursors if necessary, (3) the reactor is designed to allow a direct and fair comparison of temperature switched growth (LRP) and conventional gas flow switching. The use of organometallic (OM) arsenic sources is motivated in part by safety considerations associated with arsine. Initial experiments on the material and electrical quality of LRP-grown GaAs were hampered by the high impurity content of organometallic arsenic sources. The availability of high purity sources (such as tertiarybutylarsenic) in the past several years has enabled us to perform detailed studies in this area. Temperature switched growth of GaAs offers the prospect of more efficient use of the Column V source (lower gas flows compared to conventional techniques, for an equivalent or higher degree of interface abruptness).

Application of LRP to III-V material growth in the past three years includes the following accomplishments:

- Growth of high quality GaAs using tertiarybutylarsenic (TBAs) [*Indicates that growth of device quality GaAs is possible with TBAs.*]
- Demonstration of growth of AlGaAs/GaAs multilayer structures with abrupt, smooth interfaces, and high material quality using TBAs. [*Shows LRP is a viable growth technique for fabrication of III-V multilayer structures.*]
- Completion of a systematic comparison of GaAs growth with various OM As sources (e.g. TMAs, TEAs, TBAs) [*Provides a basis for choosing OM As sources, as well as new information about cracking mechanisms of these materials.*]
- Development of a quantitative method for extracting sheet trap density (by DLTS) for local interfacial trap concentrations which exceed the background doping. [*Required for accurate analysis of the quality of interrupted growth interfaces.*]
- Performed pressure dependent DLTS measurements on LRP samples with cooperation from Dr. G. A. Samara, Sandia National Laboratories. [*Improves current understanding of energies, capture cross-sections, and microscopic mechanisms for deep level traps in GaAs*]
- Fabrication and analysis of temperature-switched and flow-switched GaAs test samples which revealed that GaAs deposited at low temperatures is the origin of deep levels at LRP interfaces.
- Demonstration of temperature switched growth (LRP) of GaAs with high quality growth-interrupted interfaces. Deep levels can be eliminated by using fast temperature transients, and low to moderate growth rates.
- Fabrication of AlGaAs passivated MESFETs (in collaboration with Avantek) using LRP-grown GaAs and AlGaAs layers.
- Growth of conformal passivation layers of AlGaAs on mesa-isolated GaAs p⁺n diodes. [*Initial results indicate reverse leakage current reduced by a factor of two compared to untreated diodes.*]
- Investigation of various GaAs surface preparation techniques prior to deposition of passivation layers.

1.3 II-VI Highlights

A rudimentary LRP reactor was constructed in order to study heteroepitaxial growth of II-VI compound semiconductors such as ZnTe, CdTe, and ZnTe on GaAs substrates. Growth of such materials poses a number of additional difficulties compared to growth of Si or III-V layers. A variety of optical and electro-optical devices depend upon the ability to control doping, composition and thickness uniformity. Our research in this area has led us to explore a unique combination of LRP and atomic layer epitaxy (ALE) in order to achieve self-limited growth with atomic layer control. The following is a list of achievement highlights in our work on II-VI compounds:

- Demonstrated temperature-switched growth (Limited Reaction Processing) of ZnSe, CdTe, and ZnTe materials. Specular, high quality films were obtained as demonstrated by photoluminescence and RBS channeling.
- Demonstrated the ability to grow high quality (100) CdTe on (100) GaAs substrates by growing an ultra-thin ZnTe layer (20 to 100Å) on the the GaAs surface before CdTe growth. [*This shows that LRP is a viable technique for producing thin multilayer II-VI structures.*]
- Demonstrated the ability to grow high quality (111) CdTe on (100) GaAs. [*The ability to grow both orientations of CdTe on (100) GaAs has important applications in infrared detector systems (HgCdTe) and novel II-VI structures for non-linear optical devices.*]
- Achieved p-type doping of ZnTe using an arsenic organometallic, and n-type doping CdTe using trimethylindium. The Hall mobilities and carrier concentrations were found to be 14 cm²/volt-sec, 10¹⁸/cm³ and 400 cm²/volt-sec, 10¹⁶/cm³ respectively.
- Demonstrated the ability to control temperature uniformity to within +/- 3°C during growth of CdTe using a thin graphite wafer holder. [*Temperature uniformity is important in II-VI systems because of the strong dependence of growth rate and native defect concentrations on temperature.*]
- Completion of a study on the physisorption, chemisorption, and decomposition of a variety of important II-VI organometallic precursors. Characterization of these properties was obtained using the Temperature Programmed Reaction (TPR) technique. The study yielded results that are important to understanding both conventional and self-limited growth (i.e. ALE) of II-VI compounds.
- Invented and developed a new form of atomic layer epitaxy using LRP. This LRP/ALE technique was applied to the growth of II-VI compounds using organometallic precursors. We have established regimes in which growth rate is independent of concentration over a wide range of concentrations.

Part 2

List of Publications

- 2.1 C. A. King, J. L. Hoyt, C. M. Gronet, J. F. Gibbons, et al., "Characterization of p-N $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ Heterojunctions Grown by Limited Reaction Processing" *Proceedings of the 46th DRC*, June 1988.*
- 2.2 C. A. King, C. M. Gronet, J. F. Gibbons and S. D. Wilson, "Electrical Characterization of In-Situ Epitaxially Grown Si p-n Junctions Fabricated Using Limited Reaction Processing", *IEEE Electron Dev Lett.* **9** (5) pp. 229-231, May 1988.
- 2.3 J. F. Gibbons, C. A. King, J. L. Hoyt, D. B. Noble, C. M. Gronet, M. P. Scott, S. J. Rosner, S. S. Laderman, K. Nauka, J. Turner and T. I. Kamins, "Si/ $\text{Si}_{1-x}\text{Ge}_x$ Heterojunction Bipolar Transistors Fabricated by Limited Reaction Processing", *IEDM Technical Digest*, 566, (1988).
- 2.4 C. A. King, J. L. Hoyt, C. M. Gronet, J. F. Gibbons, M. P. Scott and J. Turner, "Si/ $\text{Si}_{1-x}\text{Ge}_x$ Heterojunction Bipolar Transistors Produced by Limited Reaction Processing," *IEEE Electron Dev Lett.* **10** (2) pp. 52-54, February 1989.
- 2.5 T. I. Kamins, K. Nauka, James B. Kruger, Judy L. Hoyt, C. A. King, D. B. Noble, C. M. Gronet, James F. Gibbons, "Small-Geometry, High-Performance, Si- $\text{Si}_{1-x}\text{Ge}_x$ Heterojunction Bipolar Transistors", *IEEE Electron Device Letters*, **10**, 11, pp. 503-505, November 1989.
- 2.6 T. I. Kamins, K. Nauka, L. H. Camnitz, J. B. Kruger, J. E. Turner, S. J. Rosner, and M. P. Scott, J. L. Hoyt, C. A. King, D. B. Noble, and J. F. Gibbons, "High Frequency Si/ $\text{Si}_{1-x}\text{Ge}_x$ Heterojunction Bipolar Transistors", *Proc. IEEE IEDM*, Dec. 1989, pp. 647-650.
- 2.7 C. A. King, J. L. Hoyt, J. F. Gibbons, "Bandgap and Transport Properties of $\text{Si}_{1-x}\text{Ge}_x$ by Analysis of Nearly Ideal Si/ $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ Heterojunction Bipolar Transistors", *IEEE Transactions on Electron Devices*, **36**, 10, pp. 2093-2104, October 1989.+
- 2.8 M. P. Scott, S. S. Laderman, T. I. Kamins, S. J. Rosner K. Nauka, D. B. Noble, J. L. Hoyt, C. A. King, C. M. Gronet, and J. F. Gibbons, "Onset of Misfit Dislocation Generation in As-Grown and Annealed $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ Films", *Mat. Res. Soc. Symposium Proceedings*, **130**, Thin Films: Stresses and Mechanical Properties, Editors: J. D. Braveman, W. D. Nix, D. M. Barnett and D. A. Smith, 1989, pp. 179-184.

* Best student paper award.

+ IEEE EDS Rappaport Award for best EDS paper in 1989.

- 2.9 C. A. King, J. L. Hoyt, D. B. Noble, C. M. Gronet, J. F. Gibbons, M. P. Scott, S. S. Laderman, T. I. Kamins and J. Turner "Epitaxial Growth of $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ Heterostructures by Limited Reaction Processing for Minority Carrier Device Applications," *Materials Research Society Symposium Proceedings*, Spring 1989.
- 2.10 J. L. Hoyt, C. A. King, D. B. Noble, C. M. Gronet, J. F. Gibbons, M. P. Scott, S. S. Laderman, S. J. Rosner, K. Nauka, J. Turner and T. I. Kamins, "Limited Reaction Processing: Growth of $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ for Heterojunction Bipolar Transistor Applications", *Thin Solid Films*, **184**, pp. 93-106 (1990).
- 2.11 J. F. Gibbons, J. L. Hoyt, C. A. King, D. Noble, C. Gronet, M. P. Scott, S. S. Laderman, S. J. Rosner, K. Nauka, T. Turner and T. I. Kamins "Limited Reaction Processing: Growth of Si-Ge/Si for Heterojunction Bipolar Transistor Applications", *Invited paper for Conference on Solid State Devices and Materials*, Tokyo, Japan, 1989, pp. 5-8.
- 2.12 D. B. Noble, J. L. Hoyt, and J. F. Gibbons, M. P. Scott, S. S. Laderman, S. J. Rosner, and T. I. Kamins, "Thermal Stability of $\text{Si/Si}_{1-x}\text{Ge}_x/\text{Si}$ Heterojunction Bipolar Transistor Structures Grown by Limited Reaction Processing", *Appl. Phys. Lett.* **5** (19) pp. 1978-1980, November 1989.
- 2.13 D. B. Noble, J. L. Hoyt, C. A. King, J. F. Gibbons, T. I. Kamins, and M. P. Scott, "Reduction in Misfit Dislocation Density by the Selective Growth of $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ in Small Areas", *Appl. Phys. Lett.* **56**, (1) (1990).
- 2.14 R. Hull, J. C. Bean, D. B. Noble, J. L. Hoyt and J. F. Gibbons, "Dependence of Misfit Dislocation Velocities upon Growth Technique and Oxygen Content in Strained $\text{Ge}_x\text{Si}_{1-x}/\text{Si}<100>$ Heterostructures", *Appl. Phys. Lett.*, in press.
- 2.15 D. B. Noble, J. L. Hoyt, W. D. Nix, J. F. Gibbons, S. S. Laderman, J. E. Turner and M. P. Scott, "The Effect of Oxygen on the Thermal Stability of $\text{Si}_{1-x}\text{Ge}_x$ Strained Layers", *Appl. Phys. Lett.* **58** (14), 1991.
- 2.16 D. B. Noble, J. L. Hoyt, P. Kuo, W. D. Nix, J. F. Gibbons, S. S. Laderman, J. E. Turner, S. J. Rosner, and M. P. Scott, "Thermal Stability Effects due to Oxygen in SiGe Strained Layers Grown by LRP" to be published in *Materials Research Symposium Proceedings* Spring 1991.
- 2.17 T. Ghani, J. L. Hoyt, D. B. Noble, J. F. Gibbons, J. E. Turner and T. I. Kamins, "Effect of Oxygen on Minority-Carrier Lifetime and Recombination Currents in $\text{Si}_{1-x}\text{Ge}_x$ Heterostructure Devices", *Appl. Phys. Lett.* **58** (12), pp. 1317-1319, March 25, 1991.
- 2.18 T. Ghani, J. L. Hoyt, D. B. Noble, J. F. Gibbons, J. E. Turner and T. I. Kamins "The Extraction of Minority Carrier Lifetime from the Current-Voltage Characteristics of $\text{Si/Si}_{1-x}\text{Ge}_x$ Devices" to be published in the *proceedings of Material Research Conference*, May 1991, in press.
- 2.19 T. I. Kamins, K. Nauka, R. D. Jacowitz, S. S. Laderman, J. L. Hoyt, D. B. Noble, and J. F. Gibbons, "p-n Junction Diodes in $\text{Si/Si}_{1-x}\text{Ge}_x$ Selective Epitaxial Layers", presented at *1991 Electronic Materials Conference*, Boulder, CO.

- 2.20 D. W. Vook and J. F. Gibbons, "Deep Levels and Impurities at Growth-Interrupted Interfaces: Temperature- and Gas-Switched Metalorganic Chemical Vapor Deposition of GaAs with Tertiarybutylarsenic", *J. Appl. Phys.*, **67** (4), pp. 2100-2108, February 15, 1990.
- 2.21 G. A. Samara, D. W. Vook, J. F. Gibbons, "Deep Electronic Levels at Growth Interrupted Interfaces in GaAs and the Pressure Dependence of these Levels", *submitted to J. Appl. Phys.*
- 2.22 J. C. Woicik, C. E. Bouldin, M. I. Bell, J. O. Cross, D. J. Tweet, B. D. Swanson, T. M. Zhang, L. B. Sorensen, C. A. King, J. L. Hoyt, P. Pianetta, and J. F. Gibbons, "Conservation of Bond Lengths in Strained Ge-Si Layers", *Phys. Rev. B.*, **43** (3), Jan. 1991.
- 2.23 J. L. Hoyt, D. B. Noble, T. Ghani, J. F. Gibbons, M. P. Scott, S. S. Laderman, S. J. Rosner, J. E. Turner, and T. I. Kamins, "Growth of $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ for Heterojunction Bipolar Transistor Applications", in proceedings of the *Second International Conference on Electronic Materials 1990*, edited by R. P. H. Chang, T. Sugano, and V. T. Nguyen (Material Research Society, Pittsburgh, PA, 1991), **ICEM-90**, p. 551

Part 3

List of Scientific Personnel

J. F. Gibbons, Principal Investigator
J. L. Hoyt, Research Associate

Graduate Research Assistants:

C. A. King, Ph.D received, June 1989
D. B. Noble, Ph.D received, June 1991
D. W. Vook, Ph.D received, January 1990
P. Kuo
T. Ghani
S. Hug
T. Mitchell

Part 4

Report of Inventions

1.

- A. Inventors:** J. L. Hoyt*Stanford University
C. A. King*
D. B. Noble*
J. F. Gibbons*

S. S. Laderman#Hewlett Packard, 3500 Deer Creek Rd.,
T. I. Kamins# Palo Alto, CA 94301
M. P. Scott#
- B. Title:** "Semiconductor Device Fabrication with Enhanced Thermal Stability of Structures Containing Strained Heteroepitaxial Layers".
- C. Disclosure Number:** S89-036

2.

- A. Inventors:** J. L. Hoyt*SU
D. B. Noble*
J. F. Gibbons*

T. I. Kamins#HP
M. P. Scott#
- B. Title:** "Selective and Non-Selective Deposition of $\text{Si}_{1-x}\text{Ge}_x$ on a Si Substrate that is Partially Masked with SiO_2 ".
- C. Disclosure Number:** In process